43. (Amended) A semiconductor integrated circuit device having an input circuit transmitting a signal, and a test circuit carrying out a verification of a connection of nodes, said test circuit comprising:

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a test data processing circuit processing test data for carrying out a verification of a connection of input nodes of said input circuit; and

a test input buffer, connected in parallel with said input nodes, receiving test data from said input nodes and inputting the test data to said test data processing circuit.

REMARKS

Claims 1-44 are pending in this application. By this Amendment, claims 41 and 43 are amended to more particularly point out and distinctly claim the invention. No new matter is added.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to Counsel's Deposit Account 01-2300.

Respectfully submitted,

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Enclosures: Marked-Up Copy of Amended Claims

MARKED-UP CLAIMS

41. (Amended) A test circuit that is incorporated in a device having an input circuit for inputting a signal, and that carries out a verification of a connection of nodes of said device, said test circuit comprising:

a test data generating circuit processing [generating] test data for carrying out a verification of a connection of input nodes of said input circuit; and

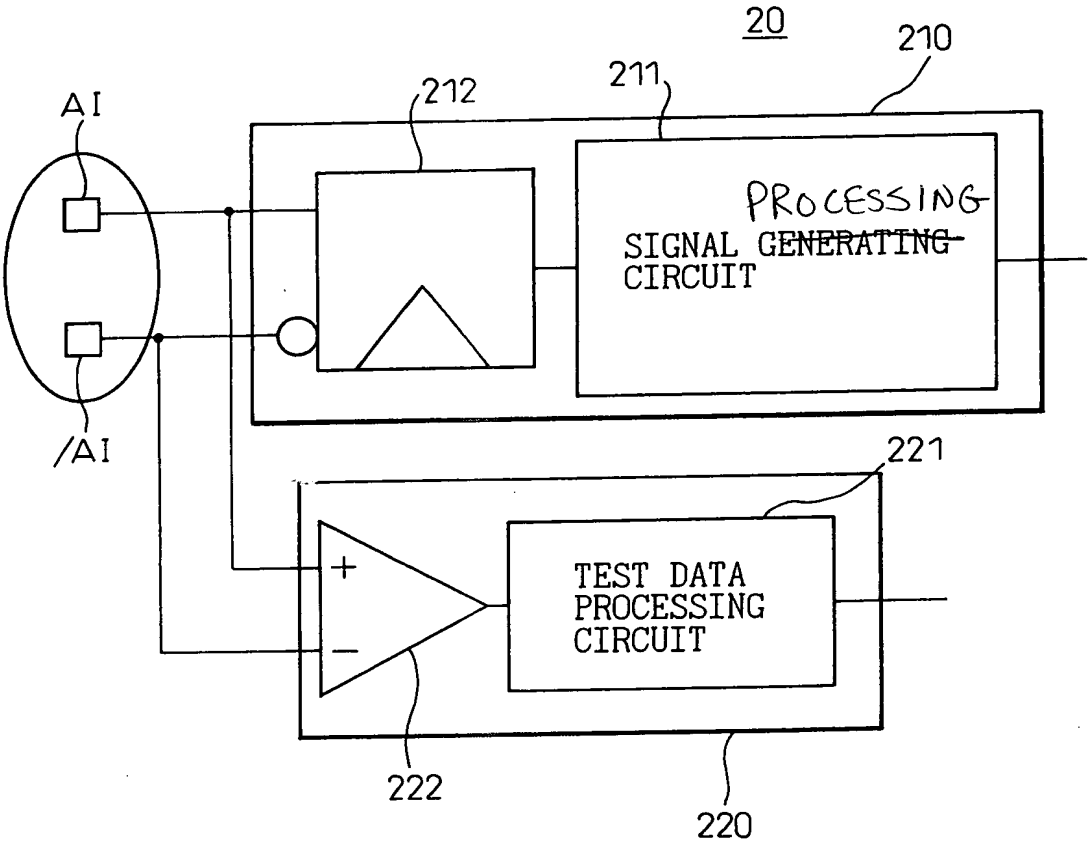
a test input buffer, connected in parallel with said input nodes, receiving test data from said input nodes [test data generating circuit] and inputting the test data to said [input nodes] test data processing circuit.

43. (Amended) A semiconductor integrated circuit device having an input circuit transmitting a signal, and a test circuit carrying out a verification of a connection of nodes, said test circuit comprising:

a test data processing [generating] circuit processing [generating] test data for carrying out a verification of a connection of input nodes of said input circuit; and

a test input buffer, connected in parallel with said input nodes, receiving test data from said input nodes [test data generating circuit] and inputting the test data to said [input nodes] test data processing circuit.

Fig.6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211
212
AI
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PROCESSING
SIGNAL GENERATING
CIRCUIT
221
TEST DATA
PROCESSING
CIRCUIT
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